

REMARKS

Claims 1-8, 10-14, 16 and 17 have been presented for examination in the Patent U.S. Patent Application.

Claims 1-8, 10-14, 16 and 17 have been rejected in the Office Action dated November 16, 2006, this rejection having been made final.

In this Continuation Application, Claim 6, 8, and 12 have been cancelled, Claims 9, and 15 having been previously cancelled.

Claims 1-5, 7, 10, 11, 13, 14, 16 and 17 are in the Continuing Application and reconsideration of the Continuing Application is hereby respectfully requested.

Referring to Paragraph 1 of the Office Action date November 16, 2006, Claims 1-3, 7, 8, 10, 14, and 16 have been rejected under 35 U.S.C. 103(a) as obvious over U.S. Patent 6,732,2061 issued in the name of Jensen et al (herein after referred to as Jensen) in view of U.S. Patent 5,870,628 issued in the name of Chen et al (hereinafter referred to as Chen). Claims 5, 6, 9, 13, and 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen, cited above, in view of Chen cited above, in further view of U.S. Patent 6,029,212 issued in the name of Kessler et al (hereinafter referred to as Kessler).

Before addressing the relationship of the references to the invention sought to be protected by the Claims, the invention defined by the Claims in the Application will be discussed. The present invention includes an interface unit for the ATM slave processing unit. This description implies that there is an ATM

1 master processor unit that is part of the complete system. The
2 signals exchanged between the ATM master processor unit and the
3 ATM slave processor unit are shown in the Figures of the
4 Application. The ATM slave processor interface unit must
5 therefore be designed to accommodate this signal exchange. In
6 particular, to minimize the apparatus required, a two-stage FIFO
7 is used both in the input section of the ATM slave processor
8 interface unit and in the output section of the ATM slave
9 processor interface unit. Notice that the two-stage input unit
10 is possible because of the difference in the clock times of the
11 bus coupling the ATM master processor and the ATM slave
12 processor. The interface unit in the ATM slave processor and in
13 the ATM master processor receives from or transmits to the bus
14 signals at a relatively slow rate. In exchanging the signals
15 from two-stage FIFO register to the remainder of the ATM
16 processor, the processor operated as a sufficient clock rate
17 relative to the bus clock rate that the two-stage FIFO register
18 can be filled or emptied by the ATM processor immediately
19 relative to the interaction with the bus.

20
21 Referring first to Jensen and the Chen references as related
22 to Claims 1, 10, and 14, the independent Claims of the
23 Application, neither these references nor the reference of
24 Kessler, disclose the interaction of an ATM slave processor unit
25 with an ATM master processor unit using the UTOPIA signal format.
26 In contradistinction, the signals exchanged between the ATM
27 master processor unit and the ATM slave processor unit using the
28 UTOPIA protocol is specifically described. The references do not
29 disclose or claim an interface unit that includes both an input
30 section and an output section. Consequently, it is believed that
31 Claims 1, 10, and 14 are patentably distinct from the Jensen,
32 Chen and Kessler reference.

1 The independent Claims or the dependent Claims dependent
2 from the independent Claims 1, 10, and 14 further include the
3 limitation of a two-stage FIFO in the input section and in the
4 output section of the interface unit. In view of this
5 difference, the Claims including this limitation are patentably
6 distinct from the references.

7
8 Referring specifically to the Jensen reference, this
9 reference includes a FIFO input register. However, as seen by
10 Fig. 1, this reference does not include a direct memory access
11 unit. In the Chen reference, a direct memory access unit is
12 shown, but the reference includes a plurality of FIFO unit. It
13 is not clear how, without the benefit of the teaching of the
14 present Application, these references can be combined. Therefore,
15 rejection of the Claims of the present Application over Jensen in
16 combination with Chen is respectfully traversed.

17
18 Dependent Claims of the present application further include
19 the limitation of the transfer of signal groups for each clock
20 cycle in a two-stage FIFO register. As indicated above, the
21 present invention recognizes that this can be accomplished with
22 both the input interface section and the output interface section
23 because of the difference in the clock rates between the system
24 bus and the direct memory access unit. This limitation is
25 patentably distinct from the disclosure teaching and claims of
26 the Jensen, Chen, and Kessler references.

27
28 Claims 2-5, 7, 11, 13, 16 and 17 all depend from either
29 Claim 1, Claim 10, or Claim 14, the independent Claims of the
30 Application. Therefore dependent Claims 2-5, 7, 11, 13, 16 and
31 17 are patentable for the same reasons that Claim 1, 10, and 14
32 are patentable.

1 Therefore, rejection of Claims 1-5, 7, 10, 11, 13, 14, 16
2 and 17 under 35 U.S.C. 103(a) over by reference to Jensen, in
3 view of Chen, in further view of Kessler is respectfully
4 traversed.
5

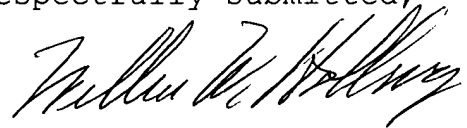
1 CONCLUSIONS

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3 In view of the foregoing amendments and the foregoing
4 discussion, it is believed that Claims 1-5, 7, 10, 11, 13, 14, 16
5 and 17 are now in condition for allowance and allowance of
6 Claims 1-5, 7, 10, 11, 13, 14, 16 and 17 is respectfully
7 requested.

8
9 Should any issues remain that can be addressed by telephone
10 interview, Examiner is respectfully requested to call the
11 undersigned attorney at 281-274-4064.

12
13 Please charge any fees in connection with the filing of this
14 amendment, including extension of time fees if any, to the Deposit
15 Account No. 20-0668 of Texas Instruments Incorporated.

16
17 Respectfully submitted,

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